AMENDMENTS TO THE SPECIFICATION

In the Specification:

Please replace paragraph number 11 with the following rewritten paragraph:

--The present invention is a method, circuit and system for determining a reference voltage. Some embodiments of the present invention relate to a system, method and circuit for establishing a set of operating reference cells to be used in operating (e.g. reading) cells in an NVM block or array. As part of the present invention, at least a subset of cells of the NVM block or array may be read using each of two or more sets of test reference cells, where each set of test reference cells may generate or otherwise provide reference voltages at least slightly offset from each other set of test reference cells. For each set of test reference cells used to read at least a subset of the NVM block, a read error rate may be calculated or otherwise determined. A set of test reference cells associated with a relatively low read error rate may be selected as the set of operating reference cells to be used in operating (e.g. reading) other cells, outside the subset of cells, in the NVM block or array. In a further embodiment, the selected set of test reference cells may be used to establish an operating set of reference cells having reference voltages substantially equal to those of the selected test set. --

Please replace paragraph number 21 with the following rewritten paragraph:

--The present invention is a method, circuit and system for determining a reference voltage. Some embodiments of the present invention relate to a system, method and circuit for establishing a set of operating reference cells to be used in operating (e.g. reading) cells in an NVM block or array. As part of the present invention, at least a subset of cells of the NVM block or array may be read using each of two or more sets of test reference cells, where each set of test reference cells may generate or otherwise provide reference voltages at least slightly offset from each other set of test reference cells. For each set of test reference cells used to read at least a subset of the NVM block, a read error rate may be calculated or otherwise determined. A set of test reference cells associated with a relatively low read error rate may be selected as the set of operating reference cells to be used in operating (e.g. reading) other cells, outside the subset of cells, in the NVM block or array. In a further

embodiment, the selected set of test reference cells may be used to establish (e.g. program) an operating set of reference cells having reference voltages substantially equal to those of the selected test set. --

Please replace paragraphs number 23-24 with the following rewritten paragraphs:

--The data read at block 320 may be used to determine a read error rate associated with the n^{th} set of test reference cells (block 330). According to some embodiments of the present invention, at least a subset of the NVM block may be a predefined portion or segment of the NVM block where source data is stored on the NVM cells along with extra error detection data/codes derived during programming. The read error rate may be determined using a variety of error rate sampling and/or error detection techniques, for example, parity bit, checksum, CRC and various other techniques. Any error detection coding and/or evaluation technique, presently known or to be devised in the future, may be applicable to present invention. --

--Once an error rate is calculated or otherwise determined for at least a subset of the NVM block using the n^{th} set of test reference cells, the error rate associated with the n^{th} set of test reference cells may be recorded (block 340). The counter 'n' may then be incremented by 1 (block 350), and the counter may be checked to see whether the new 'n' is equal to N+1, a value greater than the total number of test reference cell sets (block 360). In case that the new 'n' is smaller (not equal) than N+1 blocks 320 – 360 may be repeated, and thus an error rate associated with the use of each of the test reference cell sets to read at least a subset of the NVM block may be determined and recorded. --

Please replace the Abstract (paragraph number 42) with the following rewritten paragraph:

--The present invention is a method, circuit and system for determining a reference voltage. Some embodiments of the present invention relate to a system, method and circuit for establishing a set of operating reference cells to be used in operating (e.g. reading) cells in an NVM block or array. As part of the present invention, at least a subset of cells of the NVM

block or array may be read using each of two or more sets of test reference cells, where each set of test reference cells may generate or otherwise provide reference voltages at least slightly offset from each other set of test reference cells. For each set of test reference cells used to read at least a subset of the NVM block, a read error rate may be calculated or otherwise determined. A set of test reference cells associated with a relatively low read error rate may be selected as the set of operating reference cells to be used in operating (e.g. reading) other cells, outside the subset of cells, in the NVM block or array. In a further embodiment, the selected set of test reference cells may be used to establish an operating set of reference cells having reference voltages substantially equal to those of the selected test set. --